What is claimed is:

1. A semiconductor device comprising:

a first semiconductor chip which has a first surface;

an external connecting terminal which is formed on said first surface and which has a primary height with respect to said first surface;

a second semiconductor chip which is mounted on said first surface through a bump and which has a secondary height with respect to said first surface; and

said secondary height is smaller than said primary height.

2. A semiconductor device comprising:

a first semiconductor chip which has a first surface;

an external connecting terminal which is formed on said first surface and which has a primary height with respect to said first surface;

a second semiconductor chip which is mounted on said first surface through a bump and which has a secondary height with respect to said first surface;

a rewiring which electrically connects said first semiconductor chip, said second semiconductor chip, and said external connecting terminal with each other and which is located on said first surface; and

said second semiconductor chip being processed thin so that said secondary height being smaller than said primary height.

3. A semiconductor device comprising:

a first semiconductor chip which has a first surface;

an external connecting terminal which is formed on said first surface and which has a primary height with respect to said first surface;

a second semiconductor chip which is mounted on said first surface through a bump and which has a secondary height with respect to said first surface;

a rewiring which electrically connects said first semiconductor chip, said second semiconductor chip, and said external connecting terminal with each other and which is located on said first surface;

an insulating layer which is overlaid on said rewiring and which has predetermined opening portions in a first region for forming said external connecting terminal and in a second region for mounting said second semiconductor chip, respectively;

bedding electrodes which are formed in said predetermined opening portions, respectively, said external connecting terminal being consisting of BGA and being positioned on said bedding electrode in said first region, said second semiconductor chip being flip chip bonded to said bedding electrode in said second region through said bump; and

said second semiconductor chip being processed thin so that said secondary height being smaller than said primary height.

4. A semiconductor device as claimed in claim 3, wherein said insulating layer is made of at least two resins of which elastic

characteristics are different from each other, one resin being in said first region while another resin being in said second region.

5. A semiconductor device as claimed in claim 3, wherein both said bedding electrode in said first region and said bedding electrode in said second region are made of the same material provided in the same process.

6. A semiconductor device as claimed in claim 4, wherein both said bedding electrode in said first region and said bedding electrode in said second region are made of the same material provided in the same process.

7. A semiconductor device as claimed in claim 3, wherein said bedding electrode in said first region and said bedding electrode in said second region are made of different materials from each other.

8. A semiconductor device as claimed in claim 4, wherein said bedding electrode in said first region and said bedding electrode in said second region are made of different materials from each other.

9. A semiconductor device as claimed in claim 6, wherein a film including a material different from that of said bedding electrode is stacked on said bedding electrode.

10. A semiconductor device as claimed in claim 8, wherein a

film including a material different from that of said bedding electrode is stacked on said bedding electrode.

11. A semiconductor device as claimed in claim 1, wherein said second semiconductor chip further comprises a projection on another surface thereof opposite to a junction surface mounted to said first semiconductor chip, said projection having a ternary height with respect to said another surface of said second semiconductor chip; and said ternary height being determined so that said primary height being substantially equal to the sum of said secondary height and said ternary height.

12. A semiconductor device as claimed in claim 11, wherein said projection is made of a material selected from the group consisting of metal, conductive resin, and insulating resin.

13. A semiconductor device as claimed in claim 11, wherein said junction surface of said second semiconductor chip mounted to said first semiconductor chip through said bump is sealed by resin.

14. A semiconductor device as claimed in claim 3, further comprising a resin layer which is provided on said bedding electrode in said first region and which includes via hole penetrating to the bedding electrode in said first region, and a conductor which is buried into said via hole, and which electrically connects said external connecting terminal with the bedding electrode in said first region.

15. A semiconductor device as claimed in claim 1, wherein said first semiconductor chip comprises a member selected from the group consisting of a semiconductor chip, a function device, and an electronic component.

16. A semiconductor device as claimed in claim 1, wherein said second semiconductor chip comprises a member selected from the group consisting of a semiconductor chip, a function device, and an electronic component.

17. A semiconductor device as claimed in claim 1, wherein said second semiconductor chip comprises a plurality of chips combining a member selected from the group consisting of a semiconductor chip, a function device, and an electronic component.

18. A semiconductor device as claimed in claim 1, wherein said second semiconductor chip is processed thin by the use of at least one method selected from the group consisting of grinding, polishing, wet etching and dry etching.

19. A method of manufacturing a semiconductor device, said method comprising the steps of:

preparing a first semiconductor chip which has a first surface;

preparing an external connecting terminal which is formed on said first surface and which has a primary height with respect to said first surface;

preparing a second semiconductor chip which is mounted on said first surface through a bump and which has a secondary height with respect to said first surface; and

processing said second semiconductor chip thin so that said secondary height be smaller than said primary height.

20. A method of manufacturing a semiconductor device, said method comprising at least the steps of:

preparing a first wafer on which a plurality of first semiconductor chips each having a first region for forming an external connecting terminal and a second region for mounting a second semiconductor chip;

forming a rewiring which electrically connects said first semiconductor chip, said second semiconductor chip, and said external connecting terminal with each other and which is located on said first surface;

overlaying an insulating layer on said rewiring;

forming opening portions both in said first region for forming said external connecting terminal and in said second region for mounting said second semiconductor chip;

forming bedding electrodes in said opening portions, respectively;

carrying out a first processing for forming a bump on each of said second semiconductor chips and a second processing for dicing said second wafer to be divided into each of said second semiconductor chips, either said first processing and said second processing being able to be carried out previously;

flip chip bonding each of said second semiconductor chips

on each of said first semiconductor chips with being positioned one by one in each of said first semiconductor chips on said first wafer;

sealing junction surfaces by bumps of said second semiconductor chips by resin;

processing the under surface of said second semiconductor chip thin so that said secondary height be smaller than said primary height;

forming said external connecting terminal of BGA on each of said first semiconductor chips on said first wafer; and

dicing said first wafer to be divided into pieces.

21. A method of manufacturing a semiconductor device, said method comprising at least the steps of:

preparing a first wafer on which a plurality of first semiconductor chips each having a first region for forming an external connecting terminal and a second region for mounting a second semiconductor chip on a first surface thereof;

forming a rewiring which electrically connects said first semiconductor chip, said second semiconductor chip, and said external connecting terminal with each other and which is located on said first surface of said first semiconductor chip;

overlaying an insulating layer on said rewiring;

forming opening portions both in said first region for forming said external connecting terminal and in said second region for mounting said second semiconductor chip;

forming bedding electrodes in said opening portions, respectively;

carrying out a primary processing for forming a bump on

each of said second semiconductor chips on said second wafer, a secondary processing for processing the under surface of said second semiconductor chip thin so that, after each of said second semiconductor chips is mounted on each of said first semiconductor chips, a secondary height of each of said second semiconductor chips be smaller than a primary height of said external connecting terminal both height being with respect to said first surface of said first semiconductor chip, and a ternary processing for dicing said second wafer to be divided into each of said second semiconductor chips, said primary processing, said secondary processing, and said ternary processing being able to be carried out in any order;

flip chip bonding each of said second semiconductor chips on each of said first semiconductor chips with being positioned one by one in each of said first semiconductor chips on said first wafer;

sealing junction surfaces by bumps of said second semiconductor chips by resin;

processing the under surface of said second semiconductor chip thin so that said secondary height be smaller than said primary height;

forming said external connecting terminal of BGA on each of said first semiconductor chips on said first wafer; and

dicing said first wafer to be divided into pieces.

22. A method as claimed in claim 20, further comprising the steps of:

forming, after said processing step for processing the under surface of said second semiconductor chip thin, a

projection on said under surface, said projection having a ternary height with respect to said under surface of said second semiconductor chip, said ternary height being determined so that said primary height being substantially equal to the sum of said secondary height and said ternary height.

23. A method as claimed in claim 21, further comprising the steps of:

forming, after said sealing step for sealing junction surfaces by bumps of said second semiconductor chips by resin, a projection on said under surface, said projection having a ternary height with respect to said under surface of said second semiconductor chip, said ternary height being determined so that said primary height being substantially equal to the sum of said secondary height and said ternary height.

24. A method as claimed in claim 20, further comprising the steps of:

forming, before said forming step for forming said external connecting terminal on each of said first semiconductor chips on said first wafer, via on said bedding electrode in said first region, said via electrically connecting said external connecting terminal with the bedding electrode in said first region.

25. A method as claimed in claim 19, wherein said processing step for processing said second semiconductor chip thin includes at least one step selected from the group consisting of grinding, polishing, wet etching and dry etching.